What is claimed is:

1. A self refresh control apparatus, for use in a semiconductor memory device, comprising:

a self refresh entry unit having at least one clock buffer for generating a self refresh entry signal in response to an external control signal, wherein the clock buffer generates a clock signal in response to an external clock signal and a clock buffer enable signal;

a self refresh exit unit for generating a first self refresh exit signal in response to the external control signal and generating a second self refresh exit signal synchronized with the clock signal;

a clock buffer controller for generating the clock buffer enable signal in response to the first self refresh exit signal; and

a self refresh signal generator for generating a self refresh signal in response to the self refresh entry signal and the second self refresh exit signal.

2. The self refresh control apparatus as recited in claim 1, wherein the self refresh entry signal is synchronized with the external clock signal.

3. The self refresh control apparatus as recited in claim 2, wherein the second self refresh exit signal is synchronized with the external clock signal.

4. The self refresh control apparatus as recited in claim 1, wherein the self refresh entry unit includes:

a command buffer for receiving a plurality of command signals to output a plurality of internal command signals;

a first clock enable buffer for receiving the external control signal to output an internal clock enable signal;

a clock buffer for receiving the external clock signal and the clock buffer enable signal in order to generate the clock signal; and

a self refresh entry command generator for generating the self refresh entry signal in response to the clock signal, the internal clock enable signal and the plurality of internal command signals.

5. The self refresh control apparatus as recited in claim 1, wherein the self refresh exit unit includes:

a second clock enable buffer for generating the first self refresh exit signal in response to the external control signal;

a next clock generator for generating a pulse signal synchronizing with the second clock of the clock signal; and

a synchronizing circuit unit for generating the second self refresh exit signal by synchronizing the first self refresh exit signal with the pulse signal.

6. The self refresh control apparatus as recited in claim 1, wherein the clock buffer controller includes:

a first input unit for generating a reset signal in response to the first self refresh exit signal;

a second input unit for generating a set signal in response to the second self refresh exit signal, the self refresh signal and the pulse signal;

an RS-LATCH which receives the set signal and the reset signal; and

an output unit for generating the clock buffer enable signal in response to an outputted signal from the RS-LATCH and the self refresh signal.

7. A self refresh control apparatus included in a semiconductor memory device, comprising:

a self refresh entry unit for generating a self refresh entry signal;

a clock buffer controller for disabling a clock buffer included in the self refresh entry unit during a self refresh operation, and for enabling the clock buffer if a self refresh exit control signal is activated during the self refresh operation;

a self refresh exit unit for generating a self refresh exit signal by synchronizing the self refresh exit control signal with a pulse signal outputted from a next clock signal included in the self refresh exit unit; and

a self refresh signal generator for generating a self refresh signal for determining a period of the self refresh operation,

wherein the self refresh control apparatus controls start or end of the self refresh operation by using single clock buffer.

8. The self refresh control apparatus as recited in claim 7, wherein the self refresh exit unit includes:

a clock enable buffer for outputting the self refresh exit control signal during the self refresh operation;

the next clock generator for generating the pulse signal by detecting the second clock of an outputted clock signal from the clock buffer; and

a synchronizing circuit unit for generating the self refresh exit signal by synchronizing the self refresh exit signal from the clock enable buffer with the pulse signal from the next clock generator.

9. The self refresh control apparatus as recited in claim 8, wherein the clock buffer controller includes:

a first input unit for generating a reset signal by detecting transition point of the self refresh exit control signal outputted from the clock enable buffer;

a second input unit for generating a set signal in response to the self refresh exit signal, the self refresh signal and the pulse signal;

an RS-LATCH which receives the set signal and the reset signal; and

an output unit for generating a buffer control signal

for controlling the clock buffer in response to an outputted signal from the RS-LATCH and the self refresh signal.

10. The self refresh control apparatus as recited in claim 8, wherein the next clock generator includes:

an input unit for transferring the outputted clock signal from the clock buffer if the self refresh exit signal becomes inactivated;

a means for generating a toggle signal which toggles at a rising edge of an outputted signal from the input unit; and

an output unit for generating the pulse signal by synchronizing with an falling edge of the toggle signal.

11. The self refresh control apparatus as recited in claim 7, the self refresh entry unit includes:

a command buffer which receives a plural number of control signal operating during normal operation;

a first clock enable buffer which receives a clock enable signal operating during normal operation;

a clock buffer for receiving a clock signal; and

a self refresh entry command generator for generating a self refresh entry signal in response to outputted signals from the command buffer, the first clock enable buffer and the clock buffer.

12. A self refresh control method for a semiconductor memory device, comprising a step of:

generating a self refresh entry signal by synchronizing it with an external clock signal outputted from a clock buffer;

disabling the clock buffer at a self refresh operation;

transferring a clock enable signal to inside of the semiconductor memory device;

enabling the clock buffer if the clock enable signal is activated during the self refresh operation; and

generating a self refresh exit signal by synchronizing the clock enable signal with an outputted signal from the clock buffer.

13. The self refresh control method as recited in claim 12, further includes a step of generating a signal for determining a period of the self refresh operation by using the self refresh entry signal and the self refresh exit signal.

14. The self refresh control method as recited in claim 13, wherein the step of generating the self refresh exit signal further includes a step of:

generating a pulse signal by detecting a rising edge of the second clock of the outputted signal from the clock buffer; and

generating the self refresh signal by synchronizing the clock enable signal with the pulse signal.